REMARKS

The Office Action of June 14, 2002 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested.

Claims 1-22 are pending, claims 1 and 3 having been amended and claims 10-22 having been added.

Claims 1-9 stand rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 1-12 of U.S. Patent No. 6,373,327. Applicant respectfully traverses the rejection.

As stated on page 1 of the specification, the present application is a divisional of U.S. patent application serial No. 09/656,381. Applicant respectfully reminds the Examiner that a restriction requirement was mailed on July 25, 2001 for parent application No. 09/656,831, which issued as U.S. Patent No. 6,373,327 on April 16, 2002. Claims 1-9 of the present application correspond to non-elected claims 4-5, 12, 17, 22, 27, 32, 34 and 42 of parent application No. 09/656,831. Applicant respectfully refers the Examiner to M.P.E.P., section 804.01, which states that the third sentence of 35 U.S.C. 121 prohibits the use of a patent issuing on an application with respect to which requirement for restriction has been made, or an application filed as a result of such a requirement, as a reference against any divisional application, if the divisional application is filed before the issuance of the patent. For at least this reason, Applicant respectfully requests that the rejection be withdrawn.

Claim 3 stands rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. In particular, the Examiner indicated that in claim 3, it is unclear from where the "second voltage" is generated. Applicant submits that amended claim 3 obviates the rejection.

Amended claim 3 now recites that the second voltage is of the gate of the third transistor. Applicant submits that amended claim 3 is now definite and respectfully requests that the rejection be withdrawn.

Claims 1 and 3-6 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 5,059,815 to Bill et al. (Bill). Applicant respectfully traverses the rejection.

Amended claim 1 and claims 3-6 are directed to a voltage generating/transferring circuit comprising a first transistor connected between an input node and a node for receiving a first voltage, wherein a gate of the first transistor is connected to an input portion of one of a plurality of boost units.

To show the invention of claim 1, the action relies on Figure 1A of Bill. However, Figure 1A of Bill does not disclose, teach or suggest a gate of the first transistor connected to an input portion of one of the boost units, as recited in amended claim 1 and claims 3-6.

Applicant submits that Bill does not disclose a voltage generating/transferring circuit having each and every limitation of claims 1 and 3-6. Therefore, these claims are not anticipated by Bill and Applicant respectfully requests that the rejection be withdrawn.

Claims 2 and 7-9 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bill. Claims 2,7 and 9 ultimately depend from claim 1 and are allowable at least for the same reasons discussed above. Therefore, Applicant respectfully requests that the rejection be withdrawn.

New claims 10-22 are fully supported by the specification and are patentable over Bill for at least the reasons discussed above.

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

CONCLUSION

All rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: September 13, 2002

By: Richard C. Irving 38499
for Gary D. Fedorochko
Registration No. 35,509

1001 G Street, N.W.
Washington, D.C. 20001-4597
(202) 508-9100

GDF/RCI:lab

MARKED-UP VERSION OF AMENDED CLAIMS

1. (Amended) A voltage generating/transferring circuit comprising:

a boost unit group including a plurality of boost units series-connected between input and output nodes;

a first transistor connected between the input node and a node for receiving a first voltage; and

a first capacitor connected to the output node,

wherein each boost unit has input and output portions, ~~and includes~~ a second transistor having a gate and a drain connected to the input portion and a source connected to the output portion, and a second capacitor in each boost unit connected to the input portion, and a gate of said first transistor is connected to the input portion of one of the boost units~~output node~~.

3. (Amended) A voltage generating/transferring circuit according to claim 1, further comprising:

a third transistor which has a gate connected to the output node, and transfers a third voltage,

wherein a second voltage of the gate of said third transistor is equal to, or larger than a sum of the third voltage and a threshold voltage of said third transistor.

Claims 10-22 were added.